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Docket No. 200314976-1

Remarks

This Amendment is responsive to the **August 11, 2006** Office Action. Reexamination and reconsideration of **claims 1-24** is respectfully requested.

Summary of The Office Action

Claims 1-24 were rejected under 35 U.S.C §101 because the claimed invention is purportedly directed to non-statutory subject matter. Arguments concerning the highly controversial and much criticized Interim Guidelines are provided to rebut this rejection.

Claims 1-13 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 12, and 13 have been amended.

Claims 1-4, 6-21, and 23-24 were rejected under 35 U.S.C. §102(e) as being anticipated by Bhatia et al. (US Patent No. 6,535,798 B1)(Bhatia). Bhatia teaches a "true reactive" throttling system while the claims concern a system that simulates processor states.

Claims 5 and 22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Bhatia.

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Objections to the Drawings

The Office Action indicates that Figures 1-8 should be designated by a legend such as -- Prior Art -- because they purportedly illustrate only that which is old. Applicant respectfully disagrees since the figures illustrate systems and methods associated with simulating a processor state by selecting a stored bit pattern and then writing the selected bit pattern to an ACPI throttling register while the prior art teaches only "true reactive" systems that work in processors having both variable voltage sources and variable frequency clocks, where the "true reactive" systems neither select nor write bit patterns.

The Amendments

Claims 1, 12, and 13 have been amended to address the informalities identified in the Office Action. Specifically, the language "may be written" has been changed to "capable of being written". Thus, the purported indefiniteness has been cured without adding any new subject matter.

Claims 7 and 10 have been amended to make clear that in these claims the processor for which the processor state is simulated does not include a variable voltage source or a variable frequency clock. Support for these limitations is found in at least [0035]. Thus, no new matter has been added.

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35 U.S.C. §101

Claims 1-24 were rejected under 35 U.S.C. §101 as purportedly being directed to non-statutory subject matter. The Office Action asserts that "software per se" is not patentable. The Office Action also characterizes software as being a "judicially created exception." The Office Action recites that "the current focus of the Patent Office in regard to statutory inventions under 35 U.S.C. §101 for method claims and claims that recite a judicial exception (software) is that the claimed invention recite a practical application." Applicant notes that statutes and case law control patent law, not the "current focus of the Patent Office." When the Patent Office seeks to invent new bases for rejections, courts consistently reject these attempts. See, for example, Ex parte Lundgren, Appeal No. 2003-2088 (BPAI 2005), where the "technological arts test" created by the Patent Office was rejected. Ex parte Lundgren makes clear that the PTO must follow the law and not create the law. The law is that software is patentable.

Furthermore, the claims withstand even this incorrect application of the law by the Office Action. The claimed invention passes the practical utility test because it provides a useful, concrete, and tangible result by changing the providing of a clock signal to a processor to simulate changing a processor state. The result is useful because it facilitates actions like thermal control. The result is concrete (e.g., repeatable) because selecting a bit pattern from the data structure and writing the selected bit pattern to the ACPI throttling register will produce the throttling result in a repeatable fashion. The result is tangible (e.g., discernible, measurable) and can be easily detected using, for example, a protocol analyzer, a logic probe, or an oscilloscope. Thus the claims survive even in light of the erroneous interpretation of 35 U.S.C. §101.

The Office Action also rejects claims 22 and 24 because a computer-readable medium as described in the specification might be a transmission media such as electromagnetic radiation (e.g., wave). The Office Action recites that "the office feels" that this "does not fall into a category of invention." Once again, statues and case law control patent prosecution, not the "feelings" of the Office.

While this type of 35 U.S.C. §101 rejection may have been valid before In re Beauregard, 53 F. 2d 1583, 35 USPQ 2d 1382 (Fed. Cir. 1995), and before in re Lowry, 32 F.

3d 1579, 32 USPQ 2d 1031 (Fed. Cir. 1994) it is clearly out of place and improper now. The teachings of these cases and the PTO response to the teachings were initially provided to examiners and practitioners alike in the 1996 guidelines for examining computer related inventions. More recently, the "Interim Guidelines" were provided by the PTO in a misplaced attempt to overrule the Federal Circuit. As has been proven again and again, most recently in Ex parte Lundgren, Appeal No. 2003-2088 (BPAI 2005), the PTO must follow the law, and not create the law.

The guidelines as recited in MPEP §2106 provide guidance for how to examine computer-readable medium claims. MPEP §2106 distinguishes proper 35 U.S.C. §101 rejections for claims to forms of energy from improper 35 U.S.C. §101 rejections for claims to signals functioning as a computer-readable medium. MPEP §2106 reads, in pertinent parts:

> Claims that recite nothing but the physical characteristics of a form of energy, such as a frequency, voltage, or the strength of a magnetic field, define energy or magnetism, per se, and as such are non-statutory natural phenomena. O'Reilly v. Morse, 56 U.S. (15 How.) 62, 112-14 (1853). However, a signal claim directed to a practical application of electromagnetic energy is **statutory regardless of its transitory nature**. See O'Reilly, 56 U.S. at 114-19; In re Breslow, 616 F.2d 516, 519-21, 205 USPQ 221, 225-26 (CCPA 1980). ... In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and **is thus statutory**. (emphases added)

The 1996 guidelines were supplemented with the 1996 PTO training materials related to examining computer related inventions. These training materials discuss, with approval, this claim in US patent 5,568,202 (Koo).

> An electronic reference signal in a system for minimizing the effects of ghosts occurring during the transmission and reception of a television signal over a communications path, **wherein said reference signal is embodied in a processor readable memory**, is non-cyclic, has a substantially flat frequency response within the bandwidth of said communications path and has a plurality of substantially uniform amplitude peaks over a time interval, and wherein a replica of said reference signal is transmitted as part of said

television signal and is utilized by a decoder to derive coefficients which are used with at least one filter to remove said ghosts.

Thus, since at least 1996, this type of claim has been regarded favorably by the PTO and has been deemed to be statutory subject matter. For several years the PTO followed the law as established by the Federal Circuit in Beauregard and Lowry, which established that data structures and computer programs stored on floppy disks were statutory subject matter. The rationale behind the decisions was that a provider of infringing software should be liable as a direct infringer rather than as a contributory infringer. If the data structure or computer program on the floppy disk was not statutory, then only the user of the software would be a direct infringer. The user could end up as an unwitting infringer while the knowingly infringing provider goes free. Thus, patent owners would be forced to sue unwitting infringers for direct infringement to be able to get to the contributory infringer. If the disk were not an infringing article of manufacture and the disk was provided from outside the United States then the provider might not have even been liable for contributory infringement since they would not have made, used, sold, or imported an infringing article. This is inequitable and thus the Federal Circuit acted, making programs and data structures embodied in computer-readable mediums statutory subject matter.

However, in 2005 the PTO decided to go against the Federal Circuit by attempting to create its own law in the Interim Guidelines. The flaws in the Interim Guidelines are discussed below. Since Beauregard and Lowry, propagated signals have largely replaced floppy disks for software distribution. Thus, the Examination guidelines analogize with approval a propagated signal and a Beauregard claim (see 1996 guidelines, claim 13) (See also, Koo). The signal claim is directed to a manufactured transient phenomenon, like an electrical, optical, or acoustic signal that is more than just a perturbation. The manufactured transient phenomenon allows the transmission of computer executable instructions in the same way that the floppy disk of Beauregard and Lowry allow the transmission of computer executable instructions. Therefore, the claims are statutory subject matter, as determined by case law and PTO guidelines, and the 35 U.S.C. §101 rejection should be removed.

The Office Action appears to rely on the Interim Guidelines as authority for the position that a carrier wave is not statutory subject matter because it is not an article of manufacture. Contrary to the Office Action assertion, the Interim Guidelines as controlled

by Federal Circuit case law reveal that functional matter embodied on floppy disks, memories **and carrier waves** is statutory subject matter. Therefore this rejection is baseless and should be withdrawn.

MPEP §2106 (IV)(B)(1)(a) reads:

> A claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and **is thus statutory**. (emphasis added)

In this application the rejected claims concern a computer readable medium.

MPEP §2106 (IV)(B)(1)(c) reads:

> A signal claim directed to a practical application of electromagnetic energy **is statutory regardless of its transitory nature**. See O'Reilly, 56 U.S. at 114-19; In re Breslow, 616 F.2d 516, 519-21, 205 USPQ 221, 225-26 (CCPA 1980). (emphasis added)

In this application the rejected claims concern transmitting processor executable instructions, which is a practical application of electromagnetic energy. Thus, following MPEP §2106(IV)(B)(1), the claims are statutory and this rejection should be withdrawn. Nothing in the Interim Guidelines supercedes this settled case law.

The Interim Guidelines specifically address signal claims. Annex IV, Computer-Related Nonstatutory Subject Matter includes section (c), titled Electro-Magnetic Signals. This section reads, in pertinent parts:

> It does not appear that a claim reciting a signal encoded with functional descriptive material falls within any of the categories of patentable subject matter set forth in Sec. 101. ... A claimed signal has no physical structure, **does not itself perform any useful, concrete and tangible result** and, thus, does not fit within the definition of a machine. (emphasis added).

This reasoning is flawed. The claimed signals do perform a useful, concrete (reproducible), and tangible (detectable, physical) result. The claimed signals carry computer executable instructions from one point (e.g., local computer) to another point (e.g., remote

computer) in a repeatable, detectable, and useful manner. When received, the claimed signals transform the receiving machine into a newly programmed machine. Thus, all prongs of the "practical utility" test are met, making the claimed signals statutory subject matter.

This section of The Interim Guidelines recognizes that the issue is not closed:

> [F]rom a technological standpoint, **a signal encoded with functional descriptive material is similar to a computer-readable memory encoded with functional descriptive material**, in that they both create a functional interrelationship with a computer. In other words, a computer is able to execute the encoded functions, regardless of whether the format is a disk or a signal. (emphasis added).

Thus, even the Interim Guidelines recognize that these new §101 rejections are questionable. Since the rejections are questionable, the Examiner is invited to apply the "practical result" test identified in the Interim Guidelines to the claims in question. Since a practical result is unquestioned, the Examiner is encouraged to remove the rejections.

The Interim Guidelines conclude by stating:

> These interim guidelines **propose** that such signal claims are ineligible for patent protection because they do not fall within any of the four statutory classes of Sec. 101. **Public comment is sought for further evaluation of this question.** (emphasis added)

Even though the guidelines "propose" that the signal claims are ineligible for patent protection, **they do not require** that these claims be rejected. Indeed, the Interim Guidelines seek public comment, indicating that this is an open issue. The Interim Guidelines also caution the Examiner not to strictly apply the "article of manufacture" test. For example, Section IV, subsection A, instructs the Examiner that:

> Congress chose the expansive language of 35 U.S.C. Sec. 101 so as to include "anything under the sun that is made by man." Diamond v. Chakrabarty, 447 U.S. 303, 308-09, 206 USPQ 193, 197 (1980). ... [Thus], the question of whether a claim encompasses statutory subject matter should not focus on which of the four categories of subject matter a claim is

> directed to ... but rather on the essential characteristics of the subject matter, in particular, its practical utility.

In this application, the practical utility, (e.g., transmitting computer executable instructions from place to place) is undisputed. What is disputed is the propriety of the §101 rejections. Thus, Applicant respectfully requests that the §101 rejections be withdrawn so that meaningful prosecution on the merits can proceed.

The Claims Patentably Distinguish Over the References of Record

35 U.S.C. §102

For a 35 U.S.C. §102 reference to anticipate a claim, the reference must teach every element of the claim. Section 2133 of the MPEP recites:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Here, the reference does not teach simulating a processor state by selecting from bit patterns stored in a data structure and then writing those bit patterns to an ACPI throttling register whose address is also stored in the data structure. Additionally, the reference does not teach simulating the processor state in a processor that has neither a variable voltage supply nor a variable frequency clock.

Bhatia

Bhatia describes a true reactive system that works with processors that have elements including internal machine specific registers, variable voltage supplies, variable frequency clocks, and so on. Thus, Bhatia describes how to create a true processor state in a processor by manipulating one or more of the voltage and frequency of a processor.

The application describes simulating a processor state (e.g., voltage, frequency) in a processor that does not have internal machine specific registers, variable voltage supplies,

variable frequency clocks, and so on. The processor state is simulated by selectively throttling the processor by selecting and writing bit patterns to an ACPI throttling register.

Bhatia describes how a "power management module indicates (at 124) the new performance state of the processor ... by writing a pre-defined value to a control register." C12, l36-42. But where does this pre-defined value come from? And to where is it written? In the application, as claimed in claim 1, a data structure stores bit values for writing to the ACPI throttling register and the address of the ACPI throttling register. Bhatia describes storing "the location and structure of the control register" in an ACPI object C12, l51-53 along with "the number of performance states available, the core clock frequencies and supply level voltages to be used in performance states, the expected power consumption in each performance state", and so on. What is missing from the ACPI object are the claimed set of bit patterns and the logic to select between the members of the set of bit patterns to simulate a state. These bit patterns are missing because Bhatia establishes true states, it does not simulate them.

The values stored in Bhatia are the "core clock frequencies" and "supply level voltages" that can be used to control processors having variable voltage supplies and variable frequency clocks. Since those elements are not available in the processors upon which the claims operate, those types of values are not stored. Instead, values for controlling throttling are stored.

Thus, Bhatia does not anticipate the claims because it describes neither storing the claimed bit pattern nor selecting and writing the selected bit pattern.

Bhatia was cited in the background section of the application as an example of a true STOPCLK# reactive system that throttles a clock signal available to a processor in response to detecting a thermal condition. In this type of reactive system, "different events may be used to trigger performance state transition." C12 l5-6. Bhatia also describes how "a user (through a graphical user interface) may specify the performance state of the computer system." C12, l13-14. Bhatia also describes cycling between high performance states and low performance states. C2, l45-55. The cycling can be controlled by temperature sensing and generating a "thermal engage SMI" or a "thermal disengage SMI". C3, l48-52. To

perform the throttling, a clock control input (e.g., STPCLK#) is activated and deactivated according to a "preset duty cycle". C4, 18-12. Thus Bhatia is clearly a useful reference, but its use lies in understanding what the invention is not. The invention is not a true reactive system that manipulates frequency and voltage. The invention performs a processor state simulation. In Bhatia, there is no simulation achieved through bit pattern selection, rather a preset duty cycle is used.

Bhatia clearly recites that ACPI objects may be created and used. C12, 126-58. However, no mention is made of an object or data structure that stores both the address of an ACPI throttling register and bit patterns to write to the ACPI throttling register. Bit patterns are not stored because reduction of power dissipation is made in decrements of ΔP, a binary action for which no bit pattern storage is required. C9, 143-45.

35 U.S.C. §103

To establish a prima facie case of 35 U.S.C. §103 obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. MPEP 2143.01 Second, there must be a reasonable expectation of success. MPEP 2143.02 Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143.03 Additionally, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). This requirement is intended to prevent unacceptable "hindsight reconstruction" where Applicant's invention is recreated from references using the Application as a blueprint.

Here, the third criteria described in MPEP 2143.03 is not satisfied since the reference does not teach or suggest all the claim limitations. The reference does not teach simulating a processor state by selecting from bit patterns stored in a data structure and then writing those bit patterns to an ACPI throttling register whose address is also stored in the data structure. Additionally, the reference does not teach simulating the processor state in a processor that

has neither a variable voltage supply nor a variable frequency clock. Thus, none of the claims are obvious for at least this reason.

Claims will now be discussed individually..

Claim 15

This claim also describes establishing the data structure as an ACPI table in a BIOS operably connectable to the processor. In rejecting claim 22 for obviousness, the Office Action admits that Bhatia does not disclose establishing an ACPI table in a BIOS. Thus, in addition to being incorrect, this rejection is internally inconsistent with the rest of the Office Action.

Bhatia describes how "thermal management in the computer system 10 may be accomplished by other modules including software, firmware, and/or hardware modules. ... the thermal management routine may be implemented in another software layer (e.g., an OS module, device driver, BIOS routine)." C7, 155-61. While this describes how the management routine may be stored in a BIOS, it does not describe the data structure being part of the BIOS. Furthermore, it does not describe "establishing" the data structure as a table in a BIOS. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 22

Claim 22 was rejected under 35 U.S.C. §103(a) as being unpatentable over Bhatia. The Office Action admits that Bhatia does not disclose establishing an ACPI table in a BIOS. The Office Action then asserts that Bhatia discloses a data structure (e.g., ACPI table) operably connected to a BIOS and concludes that this is functionally equivalent to establishing the data structure in the BIOS. This is incorrect.

A data structure located in a BIOS may be accessible to BIOS routines at times when data structures external to the BIOS may not be accessible. One time when the external data structure may not be available is during times when throttling could be beneficial. By way of illustration, an overheating situation may make an external memory unavailable. If the ACPI table is located in the overheated memory, the BIOS would not be able to retrieve from the table the bit codes or the ACPI throttling register address. However, if the ACPI table is located in the BIOS, then the bit codes and the register address would be available. By way

of further illustration, during boot or reboot, memory may not yet be initialized. However, a BIOS may be able to run. If the table is available in the BIOS, then the BIOS may be able to simulate processor states during boot or reboot. This would be impossible if the table were located in a memory that has not yet been made accessible through the boot process. Thus, the Office Action is incorrect in asserting that the external memory taught in Bhatia is functionally equivalent to the internal BIOS table claimed. For this additional reason this claim is not obvious and is in condition for allowance.

Independent Claim 1

Claim 1 is directed to a system for simulating a processor state. Claim 1 recites a data structure that stores both bit patterns to write to an ACPI throttling register and the address of the ACPI throttling register. Claim 1 also recites selecting between the stored bit patterns and writing the selected bit pattern to the ACPI throttling register to simulate a processor state. The reference does not disclose storing bit patterns, selecting between the bit patterns, and selectively writing selected bit patterns to an ACPI throttling register to simulate a processor state.

Differences between a true processor state and a simulated processor state are discussed in [0014] of the application:

> Implementing a true processor performance state may include changing an internal clock frequency for a processor, changing a voltage at which a processor will operate and so on. Simulating a processor performance state may include using an ACPI accessible throttling register to throttle a processor. Throttling a processor may include, for example, controlling the percentage of time during which a processor clock operates and/or controlling the percentage of time during which a processor is supplied with a clock signal. In a true processor performance state, a clock frequency may change. In a simulated processor performance state, the clock frequency for the processor may remain substantially the same but the throttling register may partially and/or completely disable the clock and/or block the clock signal from being supplied to a processor thus controlling the number of clock edges seen by a processor. This facilitates simulating the frequency change associated with a true processor performance state. Thus, the frequency change is achieved without using a

> machine specific register internal to a processor as is typical in true processor performance state systems.

The effect of this simulation with respect to an operating system is discussed in [0016] of the application:

> The simulation may be transparent to the operating system. For example, the operating system may think that it has caused a processor performance state change while in reality the example systems and methods described herein have not produced a true processor performance state change but have instead throttled a clock signal to the processor to simulate a processor performance state change.

Differences between creating a true processor state and a simulated processor state are also discussed in [0035]:

> However, the processor **210** may not include internal machine specific registers, variable voltage supplies, variable frequency clocks and so on. Thus, rather than producing an actual processor performance state in the processor **210**, the system **200** may produce a simulated processor performance state by configuring the throttling register **230** to cause the processor **210** to be throttled. The processor **210** may be throttled, for example, when a signal is asserted on the STOPCLK# line.

The reference does not describe choosing between the stored bit patterns to find a bit pattern to write and then writing that bit pattern to the ACPI throttling register to simulate a state. The reference describes changing frequency and/or voltage to create an actual processor state. To the extent the reference describes using the STOPCLK# line, it does so in the context of supplying a pre-set duty cycle that implements changes at a fixed ΔP. Presumably, turning on or off the pre-set duty cycle is achieved through a single bit binary signal. Thus, the storing, selecting, and writing of bit patterns to simulate a processor state in a processor that does not have a variable voltage supply or a variable frequency clock is not recited in the reference.

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Close examination of the cited passage that purportedly teaches selecting a bit pattern shows that the selecting is not performed. C9, l12-26 read:

Text	Teaches Selecting Bit Pattern?
A clock duty cycle setting representing the current performance level Pn may be written by a thermal management module ... to a control register ... to define the percentage of maximum performance desired of the processor 12.	No
The control register is accessible by hardware control logic to control activation and deactivation of the processor's clock control input.	No
The number of register bits dedicated to store the clock duty cycle setting determines the number of different duty cycle settings that may be made by the hardware control logic.	No

Examination of the remainder of the reference likewise reveals no such teaching.

Since claim 1 recites features not taught or suggested by the reference, claim 1 patentably distinguishes over the reference. Accordingly, dependent claims 2-12 also patentably distinguish over the reference and are in condition for allowance.

Claims 2-12

These claims depends from claim 1, which has been shown to be not anticipated. Thus, these claims are similarly not anticipated.

Claim 5

Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over Bhatia. This claim describes that the data structure is an ACPI table in a BIOS configured to

facilitate controlling a processor function(s). Bhatia describes how "thermal management in the computer system 10 may be accomplished by other modules including software, firmware, and/or hardware modules. ... the thermal management routine may be implemented in another software layer (e.g., an OS module, device driver, BIOS routine)." C7, 155-61. While this describes how the management routine may be stored in a BIOS, it does not describe the data structure being part of the BIOS.

The Office Action also asserts that Bhatia discloses an ACPI table that can be operably connected to a BIOS and then concludes that this is functionally equivalent to the above limitation. This is incorrect. A table in a BIOS could be accessed by a BIOS routine at times when a memory connected to a BIOS could not. For example, a table in a BIOS may be accessed before any other portion of a system is booted, after other portions of a system have crashed, during certain interrupt processing, and so on. Thus, having a table located inside a BIOS is not functionally equivalent to having a table stored in a memory that is accessible to a BIOS. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 6

This claim depends from claim 1, which has been shown to be not anticipated and thus this claim is similarly not anticipated. Additionally, this claim recites that the set of bit patterns facilitates simulating two processor performance states. While Bhatia describes establishing two processor performance states, they are actual performance states, not simulated performance states. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 7

This claim depends from claim 1, which has been shown to be not anticipated and thus this claim is similarly not anticipated. Additionally, this claim has been amended to make clear that the processor for which the processor state is simulated does not have a variable voltage supply. For this additional reason this claim is not anticipated and is in condition for allowance.

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Claim 8

This claim depends from claim 1, which has been shown to be not anticipated and thus this claim is similarly not anticipated. Additionally, this claim recites that the set of bit patterns facilitates simulating two or more processor performance states. While Bhatia describes establishing two processor performance states, they are actual performance states, not simulated performance states. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 9

This claim depends from claim 8, which has been shown to be not anticipated and thus this claim is similarly not anticipated. Additionally, this claim recites that the set of bit patterns facilitates simulating processor performance states by throttling the processor for different percentages of time. While Bhatia describes establishing different processor performance states, they are actual performance states, not simulated performance states.

The Office Action asserts that C8, 155-61 teaches this limitation. This passage reads: "At one extreme, TC1 can be set to zero and change in performance ΔP may be completely based on the difference between T_n and T_l. According to one embodiment, ΔP may be set at 12.5% increments". While the reference describes 12.5% increments, it does not describe bit patterns that are used to establish the eight simulated processor states having the specifically called out values in the application. In Bhatia, to the extent that the specified states would be achieved, they would be achieved through means that did not include selecting a bit pattern and writing the bit pattern. More likely a signal to increase or decrease by ΔP would be provided. This signal would not specify the desired simulated state, just whether to increase or decrease performance. For this additional reason this claim is not anticipated and is in condition for allowance.

Independent Claim 12

Claim 12 is directed to a computer configured with a system for simulating a processor state. Claim 12 recites a computer that includes a data structure that stores both bit

patterns to write to an ACPI throttling register and the address of the ACPI throttling register. Claim 12 also recites selecting between the stored bit patterns and writing the selected bit pattern to the ACPI throttling register to simulate a processor state. The reference does not disclose storing bit patterns, selecting between the bit patterns, and selectively writing selected bit patterns to an ACPI throttling register to simulate a processor state. Additionally, the reference does not disclose a computer with the data structure and logic for choosing and writing.

The differences between creating a true processor state and a simulated processor state are discussed in [0035]:

> However, the processor **210** may not include internal machine specific registers, variable voltage supplies, variable frequency clocks and so on. Thus, rather than producing an actual processor performance state in the processor **210**, the system **200** may produce a simulated processor performance state by configuring the throttling register **230** to cause the processor **210** to be throttled. The processor **210** may be throttled, for example, when a signal is asserted on the STOPCLK# line.

The reference does not describe choosing between the stored bit patterns to find a bit pattern to write, then writing that bit pattern to the ACPI throttling register to simulate a state. The reference describes changing frequency and/or voltage to create an actual processor state. To the extent the reference describes using the STOPCLK# line, it does so in the context of a pre-set duty cycle that implements changes at a fixed ΔP. Thus, the storing, selecting, and writing of bit patterns to simulate a processor state in a processor that does not have a variable voltage supply or a variable frequency clock is not recited in the reference.

Close examination of the cited passage that purportedly teaches selecting a bit pattern shows that the selecting is not performed. Since claim 12 recites features not taught or suggested by the reference, claim 12 patentably distinguishes over the reference.

Independent Claim 13

Like claim 12, claim 13 is directed to a larger piece of equipment (e.g., printer) configured with a system for simulating a processor state. Claim 13 recites a data structure that stores both bit patterns to write to an ACPI throttling register and the address of the

ACPI throttling register. Claim 13 also recites selecting between the stored bit patterns and writing the selected bit pattern to the ACPI throttling register to simulate a processor state. The reference does not disclose storing bit patterns, selecting between the bit patterns, and selectively writing selected bit patterns to an ACPI throttling register to simulate a processor state, let alone doing so in a system in a printer. Furthermore, the reference does not describe a printer configured with the data structure and the logic. Since claim 13 recites features not taught or suggested by the reference, claim 13 patentably distinguishes over the reference.

Independent Claim 14

Claim 14 is directed to a method for simulating a processor state. Bhatia is directed towards systems and methods for creating true processor states. Claim 14 recites accessing a data structure to acquire a bit pattern to write to an ACPI throttling register. Bhatia recites storing true clock frequencies and voltages for processors having variable voltage sources and variable clock frequencies. Where Bhatia recites throttling, it describes changing performance by a ΔP amount achieved through a binary signal, not through writing one of a stored bit pattern. For at least these reasons claim 14 is not anticipated and is in condition for allowance.

Claims 15-21

These claims depend from claim 14, which has been shown to be not anticipated, and thus claims are similarly not anticipated.

Claim 16

This claim further characterizes establishing the data structure as an ACPI table in a BIOS operably connectable to the processor. The additional limitations include writing a set of bit patterns to the ACPI table and writing the address of the ACPI throttling register to the ACPI table. The Office Action asserts that C12, lines 40-43 disclose this limitation. However, this passage recites: "This may be performed, for example, by writing a predefined

value to a control register to indicate the new performance state." Writing a value to a control register does not teach writing both a set of bit patterns to a data structure (e.g., ACPI table) and the ACPI throttling register address to the same data structure. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 21

This claim includes the additional action of "acquiring an address of an ACPI status register" and then reading from that register. The Office Action asserts that Bhatia teaches acquiring the address in C12, lines 40-43. This passage reads: "[t]his may be performed, for example, by writing a predefined value to a control register to indicate the new performance state of the processor." Writing a value to a register has nothing to do with acquiring the address of a status register and then reading from that status register. For this additional reason this claim is not anticipated and is in condition for allowance.

Independent Claim 23

Claim 23 is a means plus function claim that includes "means for controlling a clock signal to the processor ... where controlling the clock signal simulates the processor performance state." While Bhatia may describe manipulating a clock signal, the manipulating does not simulate a processor performance state. The manipulating performed in Bhatia simply changes processor performance by a ΔP amount, which does simulate any processor state. The Office Action asserts that C9, l12-26 discloses simulating the processor state. However, this passage merely describes a clock duty cycle that represents a performance level. The performance level defines "the percentage of maximum performance desired of the processor." This does not simulate a state that would include a voltage level and a frequency level. For at least this reason this claim is not anticipated and is in condition for allowance.

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Independent Claim 24

This claim is directed to a set of application programming interfaces embodied on a computer-readable medium. The three interfaces work together to provide information to a system and to receive information from a system.

The Office Action purportedly identifies two of these three interfaces. However, one of the interfaces is identified incorrectly and both of the interfaces purportedly identified by the Office Action reside in a computing system, not together on a computer readable medium for execution by a computer component. The Office Action does not identify the interface for communicating the ACPI throttling register address data. Additionally, the Office Action characterizes C9 112-26 as identifying the interface for communicating a state data generated by applying bit pattern data to a register identified by the register address data. However, this passage describes writing to a control register, not reading from a status register.

For at least these reasons this claim is not anticipated and is in condition for allowance.

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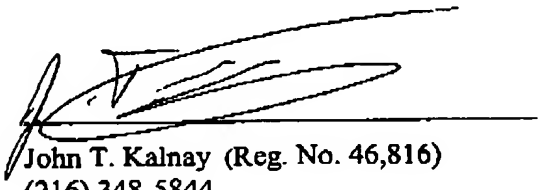
Conclusion

For the reasons set forth above, **claims 1-24** patentably and unobviously distinguish over the references and are allowable. An early allowance of all claims is earnestly solicited.

Respectfully submitted,



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